AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A simulation apparatus for simulating a very long instruction word processor, said simulation apparatus comprising:

a first simulation unit ~~operable~~configured to simulate, in a same stage in pipeline processing, execution of a group of instructions intended to be simultaneously executed, and to generate a first simulation result; and

a second simulation unit ~~operable~~configured to simulate, based on the first simulation result generated by said first simulation unit, a sequential execution of said group of instructions on an instruction-by-instruction basis, and to generate a second simulation result.

Claim 2 (Currently Amended) The simulation apparatus according to Claim 1, wherein said second simulation unit is ~~operable~~configured to generate the second simulation result by undoing the simulation of the execution of one of the instructions from said group of instructions previously simulated by said first simulation unit.

Claim 3 (Currently Amended) The simulation apparatus according to Claim 2 further comprising a display control unit ~~operable~~configured to control a display unit to display the second simulation result generated by said second simulation unit.

Claim 4 (Currently Amended) The simulation apparatus according to Claim 2, wherein said second simulation unit includes:

a judgment unit ~~operable~~configured to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions previously simulated by said first simulation;

an indication unit ~~operable~~configured to direct said first simulation unit to simulate execution of a next group of instructions when said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

a determination unit ~~operable~~configured to determine that an instruction of said group of instructions is a stop instruction when said judgment unit judges that the instruction satisfying the

break condition is included; and

a generation unit ~~operable~~configured to generate a simulation result by undoing simulations of the execution of the stop instruction and subsequent instructions in the execution of said group of instructions previously simulated.

Claim 5 (Currently Amended) The simulation apparatus according to Claim 1, wherein

said first simulation unit is ~~operable~~configured to simulate a pipeline processor that simultaneously executes a plurality of instructions, and

said simulation apparatus further comprises a display image generation unit ~~operable~~configured to generate a display image showing instructions included in a pipeline based on the first simulation results generated by said first simulation unit and the second simulation results generated by said second simulation unit.

Claim 6 (Previously Presented) The simulation apparatus according to Claim 5, wherein the display image contains a representation of an instruction included in every stage of the pipeline.

Claim 7 (Currently Amended) The simulation apparatus according to Claim 1, wherein

said first simulation unit is ~~operable~~configured to simulate, on a cycle-by-cycle basis, a pipeline processor that simultaneously executes a plurality of instructions,

said simulation apparatus further comprises:

an acception unit ~~operable~~configured to accept a user instruction for indicating a step to be executed on the instruction-by-instruction basis and for indicating a step to be executed on the cycle-by-cycle basis; and

a display image generation unit ~~operable~~configured to generate a display image showing the second simulation result generated by said second simulation unit when the user instruction that indicates the step to be executed on the instruction-by-instruction basis is accepted by said acception unit, and to generate a display image showing a simulation result generated on the cycle-by-cycle basis by said first simulation unit when the user instruction that indicates the step to be executed on the cycle-by-cycle basis is accepted by said acception unit.

Claim 8 (Previously Presented) The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction included in the pipeline.

Claim 9 (Previously Presented) The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction included in every stage of the pipeline.

Claim 10 (Currently Amended) The simulation apparatus according to Claim 1, wherein said first simulation unit includes:

a hold unit ~~operable~~configured to hold first data indicating resources of the very long instruction word processor;

a storage unit ~~operable~~configured to store a copy of the first data in a memory unit as second data; and

a first simulator ~~operable~~configured to update the first data by simulating an execution of a single group of instructions after said storage unit stores the copy of the first data,

wherein said second simulation unit is ~~operable~~configured to obtain the second simulation results of the execution of said group of instructions on the instruction-by-instruction basis based on the first data and the second data.

Claim 11 (Currently Amended) The simulation apparatus according to Claim 10, wherein

said storage unit is ~~operable~~configured to store register data in the memory unit as the second data, and

said second simulation unit is ~~operable~~configured to reconstruct data indicating a resource of the very long instruction word processor before executing the simulation of the instruction of said group of instructions on the instruction-by-instruction basis.

Claim 12 (Currently Amended) The simulation apparatus according to Claim 11, wherein said storage unit is ~~operable~~configured to store memory data, before memory writing, in said hold unit, and to store the memory data so that the memory data is contained in the second data when a memory write instruction is included in said group of instructions.

Claim 13 (Currently Amended) The simulation apparatus according to Claim 10, wherein said second simulation unit further comprises:

a judgment unit ~~operable~~configured to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

an indication unit ~~operable~~configured to direct said first simulation unit to simulate execution of a next group of instructions when said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit; and

a determination unit ~~operable~~configured to determine that an instruction is a stop instruction when said judgment unit judges that the instruction satisfying the break condition is included.

Claim 14 (Currently Amended) The simulation apparatus according to Claim 13, wherein said determination unit is ~~operable~~configured to determine that an instruction next to a present stop instruction is a break condition in a step of execution of a simulation performed on an instruction-by-instruction basis.

Claim 15 (Currently Amended) The simulation apparatus according to Claim 13, wherein said second simulation unit further comprises a reconstruction unit ~~operable~~configured to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to an instruction just prior to the stop instruction determined by said determination unit, has been simulated.

Claim 16 (Currently Amended) The simulation apparatus according to Claim 13, wherein said second simulation unit further comprises a reconstruction unit ~~operable~~configured to reconstruct, based on the first data and the second data, data indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to the stop instruction determined by said determination unit, has been simulated.

Claim 17 (Currently Amended) The simulation apparatus according to Claim 16, wherein

said first simulator is ~~operable~~configured to generate update information indicating resources of the very long instruction word processor to be changed by each instruction of said group of instructions, and

said reconstruction unit is ~~operable~~configured to reconstruct the data from the resources of the very long instruction word processor that correspond to a result of a sequential execution of the instructions of said group of instructions according to the first data, the second data, and the update information.

Claim 18 (Currently Amended) The simulation apparatus according to Claim 10, wherein

said first simulator is ~~operable~~configured to simulate an execution of the group of instructions on a cycle-by-cycle basis of pipeline processing, and

the simulation apparatus is ~~operable~~configured to count a quantity of execution cycles in the simulation for every group of instructions.

Claim 19 (Currently Amended) The simulation apparatus according to Claim 18, wherein

the very long instruction word processor to be simulated includes a cancellation unit ~~operable~~configured to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed, and

said first simulator is ~~operable~~configured to simulate said cancellation unit.

Claim 20 (Currently Amended) The simulation apparatus according to Claim 18, wherein

said first simulator is ~~operable~~configured to simulate a delay cycle according to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated, and

said reconstruction unit is ~~operable~~configured to reconstruct data indicating the resources of the very long instruction word processor that correspond to a simulation result from simulating the delay cycle according to update information for the delay instruction.

Claim 21 (Currently Amended) The simulation apparatus according to Claim 20, wherein said reconstruction unit is ~~operable~~configured to generate data indicating the resources of the very long instruction word processor that correspond to a simulation result of simulating an output dependency instruction according to the update information for the delay instruction and according to the update information for the output dependency instruction that has an output dependency in the same group of instructions as the delay instruction.

Claim 22 (Currently Amended) A simulation method for simulating a very long instruction word processor, said simulation method comprising:

performing a first simulation comprising simulating, in a same stage in pipeline processing, execution of a group of instructions comprising a plurality of instructions intended to be simultaneously executed, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation.

Claim 23 (Currently Amended) A computer-readable recording medium which stores a program for executing on a computer a simulation of a very long instruction word processor, the program causing the computer to execute a method comprising:

performing a first simulation comprising simulating, in a same stage in pipeline processing, execution of a group of instructions comprising a plurality of instructions intended to be simultaneously executed, and generating a first simulation result of said first simulation; and

performing a second simulation comprising simulating, based on the first simulation result, a sequential execution of said group of instructions on an instruction-by-instruction basis and generating a second simulation result of said second simulation.